Application No.: 09/008,497 Docket No.: 21987-00033-US

REMARKS/ARGUMENTS

Bearing in mind the comments of the final Official Action and the amendments and arguments submitted herewith, the application is now believed to be in condition for allowance. An early indication of the same would be appreciated.

Claims 1-9, 21-32, 34-38, and 39 (formerly incorrectly numbered claim 40) remain pending in this application. Claims 1, 21, 28, 31, 34, and 38 are independent. Claims 1, 21, 28, 31, 34, 38, and 40 have been amended. Claim 33 has been canceled, and no claims have been added by this Amendment.

Applicant points out that there was no claim 39 in this case, as the previous Amendment filed on March 28, 2000 inadvertently misnumbered claim 39 as claim 40. Applicant requests that claim 40 be renumbered as claim 39 to ensure consistent claim numbering in this application.

Claims 10-20 were canceled by the Preliminary Amendment on January 14, 1998, as these claims were successfully prosecuted in parent application 08/747,928, now issued as U.S. Patent No. 5,744,835.

Further, this application was unintentionally abandoned; the Petition to Revive was granted in Paper No. 16, dated November 15, 2002.

Withdrawal of the rejection of claims 1-10 and 21-40 under 35 U.S.C. §103(a) as being unpatentable over Chiu (US 4,994,402) or Matthews (US 5,134,083) and Kwon et al. (US 5,073,510), in view of Giammarco et al. (US 4,871,630) is requested. Claim 10 was previously withdrawn from consideration, as being directed to a non-elected invention.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art reference must teach or suggest all the claim***

limitations.[1] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[2]

An essential evidentiary component of an obviousness rejection is a teaching or suggestion or motivation to combine the prior art references.[3] Combining prior art references without evidence of a suggestion, teaching or motivation simply takes the inventors' disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.[4]

"There are three possible sources for a motivation to combine references: ***the nature of the problem to be solved***, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."[5] Further with regard to the level of skill of practitioners in the art, there is nothing in the statutes or the case law which makes "that which is within the capabilities of one skilled in the art" synonymous with obviousness.[6] The level of skill in the art cannot be relied upon to provide the suggestion to combine references.[7]

Applicant's disclosed and claimed invention is directed to a method for manufacturing a semiconductor device which has a buried conductive layer connected, in one embodiment, to a source or drain of a MOS transistor through a contact hole having dimensions smaller than that achievable solely by reliance upon available photolithographic processing limits. Further, in view of the sub-photolithographic feature sizes achievable by the recited method, the method of Applicant's invention is designed so as to ensure that the contact hole avoids undesirable and detrimental alignment with an associated sidewall below the contact hole, e.g., sidewalls on a gate structure, and instead generally aligns with a central portion of the device element.

One technical problem solved by Applicant's recited invention is to prevent damage to the silicon substrate due to exposure resulting from the undesirable alignment of the contact hole with the underlying sidewall below the contact hole. Prevention of damage to the underlying substrate, for example, is accomplished by ensuring that the contact hole is, in one embodiment,

---

[1] *See* MPEP §2143.
[2] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.
[3] *C.R. Bard, Inc. v. M3 Systems, Inc.*, 48 USPQ2d 1225 (Fed. Cir. 1998)
[4] *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985)
[5] *See* MPEP §2143.01, citing *In re Rouffet*, 149 F.3d, 1350, 1357, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998).
[6] *Ex parte Gerlach and Woerner*, 212 USPQ 471 (PTO Bd. App. 1980).

narrower than an underlying gate length, and is sufficiently centered above the gate structure so as to avoid registration or overlap with any associated sidewall underneath the contact hole.

Turning now to the applied art, Chiu is directed to a method of conventional fabrication of a coplanar, self-aligned contact structure in a semiconductor device. Chiu is not directed to provision of feature sizes or holes having dimensions smaller than that achievable by standard photolithographic techniques. In fact, Chiu does not teach or suggest a solution, and does not even acknowledge the technical problems associated with manufacture of semiconductor devices having sub-photolithographic feature sizes, as in Applicant's disclosed and claimed invention.

Further, ***Chiu teaches away from at least one aspect of Applicant's disclosed and recited invention***, by stating unequivocally that hole alignment is not critical. In particular, Chiu teaches that "no ill effects are suffered if one of the holes is wider than the pad which lies beneath it or slightly misaligned with respect thereto." (See Chiu at col. 7, lines 50-55). This teaching is directly contrary to at least one objective of Applicant's disclosed and claimed invention.

It is impermissible within the framework of 35 U.S.C. §103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one skilled in the art.[8] Further in this regard, As the Court of Customs and Patent Appeals, predecessor to the Federal Circuit, has held:

> All relevant teachings of cited references must be considered in determining what they fairly teach to one having ordinary skill in the art. The relevant portions of a reference include not only those teachings which would suggest particular aspects of an invention to one having ordinary skill in the art, but also those teachings which would lead such a person away from the claimed invention.[9]

Thus, Applicant submits that a person having skill in the art would not be motivated to rely upon the teachings of Chiu to solve the technical problem addressed by Applicant's disclosed and claimed invention and, therefore, Chiu is not properly combinable with any other reference for the purposes of rendering obvious Applicant's recited invention.

---

[7] *See* MPEP §2143.01, citing *Al-Site Corp. v. VSI Int'l Inc.*, 50 USPQ2d 1161 (Fed. Cir. 1999).
[8] *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 230 USPQ 416 (Fed. Cir. 1986).
[9] *In re Mercier*, 185 USPQ 774, 778 (CCPA 1975).

Matthews is directed to processes for simultaneously fabricating CMOS and bipolar transistors (i.e., "BiCMOS" devices) in the same semiconductor device. Matthews, similar to Chiu, does not acknowledge the technical problem solved by Applicant's disclosed and claimed invention relating to provision of sub-photolithographic feature sizes in a semiconductor device.

Kwon et al. is directed to a fabrication method of a contact window in a semiconductor device which can prevent an incomplete silicon exposure of the contact window by sufficient overetching insulators in the contact window formation process. Kwon et al., similar to both Matthews and Chiu, does not even acknowledge the technical problem solved by Applicant's disclosed and claimed invention relating to provision of sub-photolithographic feature sizes in a semiconductor device.

As the Federal Circuit has further noted, "[a] reference is not available under 35 **USC §103 if it is not within the field of the inventor's endeavor and was not directly pertinent to the particular problem with which the inventor was involved.**[10]

Thus, Applicant submits that neither Matthews or Kwon et al. is properly combinable with any other reference for the purposes of rendering obvious Applicant's recited invention.

The Official Action acknowledges that both Chiu or Matthews in combination with Kwon et al. are deficient by not specifically disclosing a gate electrode having a width equal to the minimum size possible with a lithographic process. The Examiner offers Giammarco et al. as making up for this deficiency.

Whether or not Giammarco et al. teaches that for which it is offered by the Official Action, Applicant submits that Giammarco et al. is not properly combinable with any of other references, i.e., Chiu, Matthews, or Kwon et al., for the purposes of rendering obvious Applicant's recited invention, as the primary references are directed to the solution of a completely different technical problem than Applicant's disclosed and claimed invention. Thus, the motivation to combine the references in the manner suggested by the Examiner is deficient.

[10] *King Instrument Corp. v. Otari Corp.*, 226 USPQ 402 (Fed. Cir. 1985).

The rejections in the Official Action amount, in substance, to nothing more than hindsight reconstruction of Applicant's invention by relying on isolated teachings of the applied art, without considering the overall context within which those teachings are presented. Without benefit of Applicant's disclosure, a person having ordinary skill in the art would not know what portions of [Chiu, Matthews, Kwon et al., and Giammarco et al.] to consider, and what portions to disregard as irrelevant or misleading.[11]

Accordingly, withdrawal of the unpatentability rejections and allowance of the pending claims is requested.

Even assuming that the references are properly combinable as suggested by the Examiner, a proposition with which Applicant disagrees for the reasons discussed above relating to lack of proper motivation, the applied art, taken alone or in combination, does not teach or suggest the recited features.

For example, the applied art, either alone or in combination, does not teach or suggest a method for manufacturing a semiconductor device having a buried conductive layer which is connected to one of a source and a drain of a MOS transistor ***and which extends over a gate electrode of said MOS transistor***, which includes, among other features, "...forming a second conductive film to be a part of said buried conductive layer on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film and said side wall insulating film formed thereon...processing said first mask layer to have a pattern which is separated into both side portions as to said first conductive film...selectively etching away said second conductive film with the patterns of said first and second mask layers as a mask so as to process said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by an openings smaller than the minimum processing size, ***and wherein said buried conductive layer extends over the gate electrode of the MOS transistor***", as recited in independent claim 1, as amended.

Further, the applied art, either alone or in combination, does not teach or suggest a method for of forming a semiconductor device using a lithographic process having a predetermined minimum processing feature size, which includes, among other features,

[11] *In re Wesslau*, 147 USPQ 391, 393 (CCPA 1965).

"...forming a conductive layer over the semiconductor element and the substrate...patterning [a] first mask layer to form a slit dividing the first mask layer into at least two mask portions, the slit having a width equal in size to the minimum processing feature size and having side walls corresponding to end faces of the two mask portions, ***wherein said side walls are formed so as to be between and offset from end portions of the semiconductor element*** [and] etching the conductive layer using the first and second mask layers to separate the conductive layer into at least two conductive layer portions, the at least two conductive layer portions being separated by a distance which is less than the minimum processing feature size", as recited in independent claim 21, as amended.

Still further, the applied art, either alone or in combination, does not teach or suggest a method of forming a semiconductor device, which includes, among other features, "...forming source and drain regions in the active area with a gate structure overlying the substrate therebetween...forming a conductive layer over the substrate and the gate structure...[and] etching the conductive layer using the first and second mask layers as a mask, thereby patterning the conductive layer into at least two portions separated by a distance which is less than a minimum processing size, wherein opposing faces of the at least two portions extend over a central portion of the gate structure", as recited in independent claim 28, as amended.

In addition, the applied art, either alone or in combination, does not teach or suggest a method of semiconductor manufacture which includes, among other features, "...patterning [a] first layer to have holes with sidewalls separated by a width equal to a minimum feature size achievable by a lithographic process used during manufacture of the device...forming a second layer on the sidewalls so as to reduce the width of the holes below the minimum feature size...patterning a conductive layer beneath the first and second layers using the holes to form openings in the conductive layer that are smaller in size than the minimum feature size, wherein the openings in the conductive layer are about 1/3 the minimum feature size", as recited in independent claim 31, as amended.

This particular aspect of this claimed invention, originally presented in dependent claim 33, and now incorporated into amended independent claim 31, is discussed in Applicant's Specification, at least at page 12, lines 16-19. This feature of maintaining the openings in the conductive layer to be about 1/3 the minimum feature size, realized in one aspect by providing

the thickness of the conductive layer as 1/3 of the width of the holes in the first layer, ensures that the area between the two portions is not completely filled with the conductive layer.

Further, the applied art, taken alone or in combination, does not teach or suggest a method of forming a semiconductor device, which includes, among other features, "...forming a gate electrode overlying the substrate between the source and drain regions, the gate electrode having a width no larger than a minimum processing size available with a photolithographic process associated with forming the gate electrode...and forming a contact hole in the first layer in an area above the gate electrode, the contact hole having a width smaller than the minimum processing size of the photolithographic process, ***said contact hole extending over at least one of the source and drain regions, and extending over only a side portion of the gate electrode***", as recited in independent claim 34, as amended.

Finally, the applied art, taken alone or in combination, does not teach or suggest a method of forming a semiconductor device, which includes, among other features, "...forming a slit in the first layer located over the structure, the slit having sidewall spacers separated by a second width, wherein the sidewall spacers are centrally arranged interior to edges of the structure...wherein the second width is smaller than a minimum feature size achievable with a lithographic process used for making the semiconductor device", as recited in independent claim 38, as amended.

As the applied art, taken alone or in combination, does not teach or suggest all the various recited features in the independent claims, reconsideration and allowance of independent claims 1, 21, 28, 31, 34, and 38 is requested.

Further, as dependent claims 2-9, 22-27, 29-30, 32, 35-37, and 39 (formerly claim 40) variously and ultimately depend from independent claims 1, 21, 28, 31, 34, and 38 and, consequently incorporate their allowable features, these dependent claims are also submitted as being allowable, without recourse to the additional patentable limitations respectively recited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment.

In view of the above, each of the presently pending claims 1-9, 21-32, 34-38, and 39 in

Application No.: 09/008,497 Docket No.: 21987-00033-US

this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

The Examiner is respectfully requested to enter this Amendment After Final, in that it raises no new issues, but merely places the claims in a form more clearly patentable over the references of record. In the alternative, the Examiner is respectfully requested to enter this Amendment After Final in that it reduces the issues for appeal.

The Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to CBLH Deposit Account No. 22-0185.

Respectfully submitted,

By Larry J. Hume

Larry J. Hume
Registration No.: 44,163
CONNOLLY BOVE LODGE & HUTZ, LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorneys for Applicant

Enclosure: Claims after Amendment

Claims after Amendment

IN THE CLAIMS:

Please cancel dependent claim 33 without prejudice or disclaimer as to the subject matter contained therein.

Please renumber dependent claim 40 as claim 39, to correct an obvious numbering error, as acknowledged in the Official Action.

Please amend independent claims 1, 21, 28, 31, 34, and 38 as follows.

1. (Twice Amended) A method for manufacturing a semiconductor device having a buried conductive layer which is connected to one of a source and a drain of a MOS transistor and which extends over a gate electrode of said MOS transistor, said method comprising ~~the steps of~~:

forming a first insulating film on a semiconductor substrate;

forming a first conductive film as said gate electrode and a second insulating film on said first insulating film, said gate electrode having a width equal to a minimum processing size achievable with a lithographic process technique;

forming a third insulating film on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film and said second insulating film formed thereon;

selectively etching away said third insulating film so as to form a side wall insulating film including said third insulating film on each of both side faces of said first conductive film and said second insulating film and also to expose said semiconductor substrate in portions which are not covered with said side wall insulating film and not covered with said first conductive film;

diffusing impurities into said exposed portions of said semiconductor substrate so as to form a source and a drain in said semiconductor substrate;

forming a second conductive film to be a part of said buried conductive layer on the whole surface of said semiconductor substrate having said first insulating film, said first

conductive film, said second insulating film and said side wall insulating film formed thereon;

forming a first mask layer on said second conductive film;

processing said first mask layer to have a pattern which is separated into both side portions as to said first conductive film;

forming a second mask layer on the whole surface of said semiconductor substrate having said first insulating film, said first conductive film, said second insulating film, said side wall insulating film, said second conductive film and said first mask layer formed thereon;

selectively etching away said second mask layer so as to leave a pattern of said second mask layer on each of both side faces of the pattern of said first mask layer; and

selectively etching away said second conductive film with the patterns of said first and second mask layers as a mask so as to process said second conductive film into a pattern in which said second conductive film is separated on said second insulating film by an openings smaller than the minimum processing size, and wherein said buried conductive layer extends over the gate electrode of the MOS transistor.

21. (Amended) A method of forming a semiconductor device using a lithographic process having a predetermined minimum processing feature size, comprising:

forming a semiconductor element in a substrate;

forming a conductive layer over the semiconductor element and the substrate;

forming a first mask layer on the conductive layer;

patterning the first mask layer to form a slit dividing the first mask layer into at least two mask portions, the slit having a width equal in size to the minimum processing feature size and having side walls corresponding to end faces of the two mask portions, wherein said side walls are formed so as to be between and offset from end portions of the semiconductor element;

forming a second mask layer on the slit sidewalls, thereby reducing the width of the slit; and

etching the conductive layer using the first and second mask layers to separate the conductive layer into at least two conductive layer portions, the at least two conductive layer

portions being separated by a distance which is less than the minimum processing feature size.

28. (Amended) A method of forming a semiconductor device, comprising:

defining an active area in a substrate;

forming source and drain regions in the active area with a gate structure overlying the substrate therebetween;

forming a conductive layer over the substrate and the gate structure;

forming a first mask over the conductive layer;

performing photolithography to form a slit in a part of the first mask layer overlying the gate structure;

forming a second mask layer on the first mask layer and in the slit;

selectively etching away the second mask layer to leave the second mask layer on side faces of the first mask layer in the slit; and

etching the conductive layer using the first and second mask layers as a mask, thereby patterning the conductive layer into at least two portions separated by a distance which is less than a minimum processing size, wherein opposing faces of the at least two portions extend over a central portion of the gate structure.

31. (Amended) A method of semiconductor manufacture comprising:

forming a first layer over a semiconductor substrate;

patterning the first layer to have holes with sidewalls separated by a width equal to a minimum feature size achievable by a lithographic process used during manufacture of the device;

forming a second layer on the sidewalls so as to reduce the width of the holes below the minimum feature size;

patterning a conductive layer beneath the first and second layers using the holes to form openings in the conductive layer that are smaller in size than the minimum feature size,

wherein the openings in the conductive layer are about 1/3 the minimum feature size.

34. (Amended) A method of forming a semiconductor device, comprising:

defining an active area in a substrate;

forming source and drain regions in the active area;

forming a gate electrode overlying the substrate between the source and drain regions, the gate electrode having a width no larger than a minimum processing size available with a photolithographic process associated with forming the gate electrode;

forming a first layer over at least the active area of the substrate; and

forming a contact hole in the first layer in an area above the gate electrode, the contact hole having a width smaller than the minimum processing size of the photolithographic process, said contact hole extending over at least one of the source and drain regions, and extending over only a side portion of the gate electrode.

38. (Amended) A method of forming a semiconductor device, comprising:

forming a structure having a first width on a substrate;

forming a first layer over at least the structure; and

forming a slit in the first layer located over the structure, the slit having sidewall spacers separated by a second width,

wherein the sidewall spacers are centrally arranged interior to edges of the structure, and

wherein the ~~first width may be minimized as the~~ second width is smaller than a minimum feature size achievable with a lithographic process used for making ~~such~~ the semiconductor device.

Please renumber claim 40 as claim 39:

~~40~~39. A method of forming a semiconductor device, comprising:

defining an active area in a substrate with isolation structures, the isolation structure

having a width no larger than a minimum processing size available with a photolithographic process associated with forming the isolation structure;

forming a first layer over at least the isolation structure; and

forming a contact hole in the first layer in an area above the isolation structure, the contact hole having a width smaller than the minimum processing size of the photolithographic process.